**Lab Number: 2**

**Section Number: ECE2411-001**

**Names: Barak Barclay**

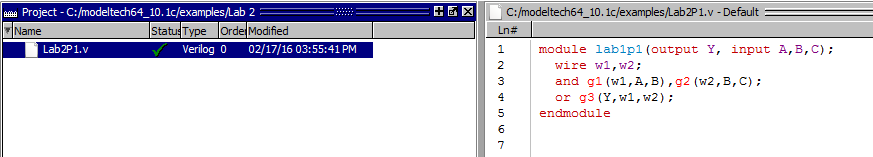
**Assigned Date: 02/11/2016**

**Due Date: 02/18/2016**

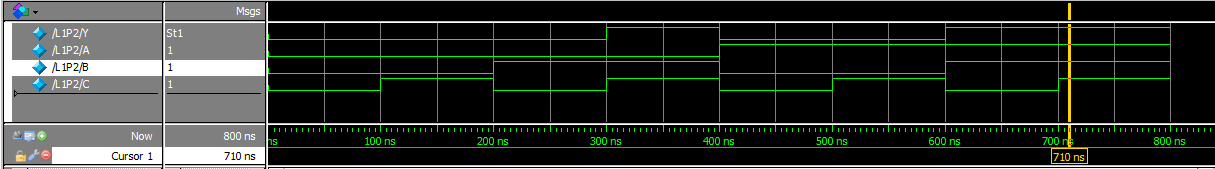
**Introduction:**

In the first part of the lab, we are given a simple circuit to create in ModelSim. Part 2 is to create a test bench for all 8 possible combinations of A, B, and C for the circuit in part 1. In part 3, two equations are given to us and we are to write a module in ModelSim using &&, || and ! that represent the equations. In part 4, we are given a circuit that includes a UDP and we are to write a module and UDP the creates it in ModelSim.

**Part 1:**



**Part 2:**



module L1P2;

wire Y;

reg A,B,C;

Lab2P1 M1(Y,A,B,C);

initial

begin

A = 1'b0;B = 1'b0;C = 1'b0;

#100 A = 1'b0;B = 1'b0;C = 1'b1;

#100 A = 1'b0;B = 1'b1;C = 1'b0;

#100 A = 1'b0;B = 1'b1;C = 1'b1;

#100 A = 1'b1;B = 1'b0;C = 1'b0;

#100 A = 1'b1;B = 1'b0;C = 1'b1;

#100 A = 1'b1;B = 1'b1;C = 1'b0;

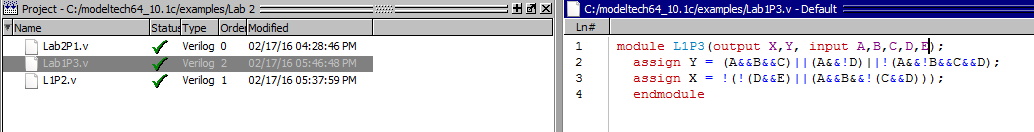
#100 A = 1'b1;B = 1'b1;C = 1'b1;

end

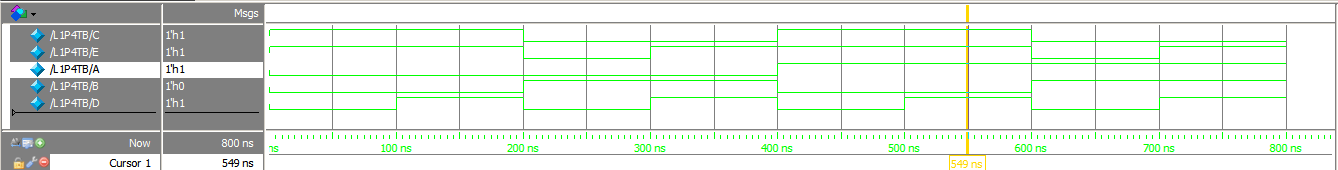
initial #800 $stop;

endmodule

**Part 3:**



**Part 4:**



module L1P4(C,E,A,B,D);

output C,E;

input A,B,D;

L1P4UDP(C,A,B);

or (E,C,D);

endmodule

primitive L1P4UDP(output C, input A,B);

table

// A B : C

0 0 : 1;

0 1 : 0;

1 0 : 1;

1 1 : 0;

endtable

endprimitive

**Conclusion:**

A module including ports, wires, and primitive gates were used to create the circuit in part 1. In part 2, a test bench module was created that included ports, a call to the module in part 1(*Lab2P1 M1(Y,A,B,C);*), values for the inputs (*A = 1'b0;*), propagation delays (*#100*), as well as other necessary code for a test bench. Part 3 was accomplished a lot like the module in part one, but instead of using primitive gates, the outputs were assigned values, noting that the “!” had to come before whatever it was NOTting. Part 4 was also accomplished a lot like the module in part 1, but one of the outputs was given a value by calling a UDP (*L1P4UDP(C,A,B);*). The UDP was made by defining a primitive that included a table.